embodiment, drain pad electrode **80** is formed to cover drain electrode **51**. By performing the steps (S**10**) to (S**110**) above, MOSFET **2** is manufactured and the semiconductor device manufacturing method according to the present embodiment is completed.

[0104] As described above, in MOSFETs **1**, **2** as the semiconductor devices according to the embodiments of the present invention above, active region **10**B and potential fixing region **10**C which is a semiconductor layer located outside active region **10**B are formed. Then, potential fixing region **10**C is electrically connected to source interconnection **60** arranged to lie over active region **10**B. Therefore, in MOSFETs **1**, **2** as the semiconductor devices according to the embodiments of the present invention above, a potential at the surface portion of the semiconductor layer located outside active region **10**B can be fixed to a potential as high as a potential of source interconnection **60**. Consequently, with MOSFETs **1**, **2** as the semiconductor devices according to the embodiments of the present invention above, the semiconductor device excellent in breakdown voltage characteristics can be provided.

[0105] In addition, with MOSFETs **1**, **2** as the semiconductor devices according to the embodiments of the present invention above, electrical connection between gate interconnection **70** arranged on potential fixing region **10**C and gate electrode **40** can readily be achieved while a potential of potential fixing region **10**C is fixed to a potential of source interconnection **60**. Then, MOSFETs **1**, **2** are different from each other in connection between potential fixing region **10**C and source interconnection **60** and connection between gate interconnection **70** and gate electrode **40**, as set forth below.

[0106] Initially, in MOSFET **1**, source interconnection **60** is electrically connected to potential fixing region **10**C without extending to potential fixing region **10**C. In addition, gate interconnection **70** is electrically connected to gate electrode **40** without extending to gate electrode **40**. Therefore, in MOSFET **1**, source interconnection **60** and gate interconnection **70** are readily arranged while a distance therebetween is maintained when viewed two-dimensionally. Consequently, according to MOSFET **1**, contact between source interconnection **60** and gate interconnection **70** can readily be avoided and short-circuiting between source interconnection **60** and gate interconnection **70** can be suppressed.

[0107] Meanwhile, in MOSFET **2**, potential fixing region **10**C is electrically connected to source interconnection **60** without extending to a portion below source interconnection **60**. Therefore, in electrical connection between potential fixing region **10**C and source interconnection **60**, potential fixing region **10**C can be formed more readily than in a case where potential fixing region **10**C is caused to extend to the portion below source interconnection **60**. In addition, gate electrode **40** is electrically connected to gate interconnection **70** without extending to a portion below gate interconnection **70**. Therefore, in electrical connection between gate electrode **40** and gate interconnection **70**, gate electrode **40** can be formed more readily than in a case where gate electrode **40** is caused to extend to the portion below gate interconnection **70**. Consequently, according to MOSFET **2**, a structure in semiconductor substrate **10** can be easier to form.

[0108] The semiconductor device and the semiconductor device manufacturing method according to the present invention can particularly advantageously be applied to a semiconductor device required to have a fixed potential at a surface portion of a semiconductor layer located outside an active region and a method of manufacturing the semiconductor device.

[0109] Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the scope of the present invention being interpreted by the terms of the appended claims.

What is claimed is:

1. A semiconductor device, comprising:
- a semiconductor substrate having a trench formed in one main surface;
- a first insulating film arranged on and in contact with a wall surface of said trench;
- a gate electrode arranged on and in contact with said first insulating film; and
- a first interconnection arranged on said one main surface,
- said semiconductor substrate including
  - a drift layer having a first conductivity type, and
  - a body layer having a second conductivity type, which is arranged on a side of said one main surface when viewed from said drift layer,
- said trench being formed to penetrate said body layer and to reach said drift layer,
- said trench including an outer peripheral trench arranged to surround an active region when viewed two-dimensionally,
- a potential fixing region where said body layer is exposed being formed in said one main surface opposite to said active region when viewed from said outer peripheral trench,
- said first interconnection being arranged to lie over said active region when viewed two-dimensionally, and
- said potential fixing region being electrically connected to said first interconnection.

2. The semiconductor device according to claim **1**, wherein
- in a region of said drift layer in contact with said outer peripheral trench, an electric field relaxing region having the second conductivity type is formed, and
- said electric field relaxing region is connected to said potential fixing region.

3. The semiconductor device according to claim **1**, further comprising:
- a second insulating film arranged above said potential fixing region; and
- a second interconnection arranged above said second insulating film, wherein
- said potential fixing region includes a potential fixing region extension portion extending to a portion below said first interconnection,
- said gate electrode includes a gate electrode extension portion extending to a portion below said second interconnection,
- said potential fixing region is electrically connected to said first interconnection in said potential fixing region extension portion, and
- said gate electrode is electrically connected to said second interconnection in said gate electrode extension portion.

4. The semiconductor device according to claim **1**, further comprising:
- a second insulating film arranged above said potential fixing region; and
- a second interconnection arranged above said second insulating film, wherein